A35056 - 066340.0144

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

On Appeal to the Board of Appeals and Interferences

Appellant(s)	:	Jens David et al.	Examiner: Thuan Du N
Serial No.	:	10/525,688	Group Art Unit: 2116
Filed	:	July 27, 2005	
Title	:	Method For Initializing Programmable System	

APPEAL BRIEF

I hereby certify that this paper is being transmitted via facsimile to the United States Patent and Trademark Office at **571-273-8300** on.

November 16, 2007
Date of Deposit

Manu J Tejwani	37,952
Attorney Name	Registration No.
Signature	November 16, 2007
	Date of Signature

TABLE OF CONTENTS

A35056 - 066340.0144

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

On Appeal to the Board of Appeals and Interferences

Appellant(s)	:	Jens David et al.	Examiner: Thuan Du N
Serial No.	:	10/525,688	Group Art Unit: 2116
Filed	:	July 27, 2005	
Title	:	Method For Initializing Programmable System	

APPEAL BRIEF

Commissioner for Patents
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On August 2, 2007, Appellants filed a Notice of Appeal from and an Pre-Appeal Brief Request for Review of the final rejection of twice-rejected claims 1-10 contained in the Office Action dated May 16, 2007. The Notice of Appeal was received by the U.S. Patent and Trademark Office on August 2, 2007. The Panel Decision from the Pre-Appeal Brief Request for Review dated October 16 2007 is to proceed to the Board of Patent Appeals and Interferences. Appellants hereby timely submit, pursuant to 37 C.F.R. § 41.37, an Appeal Brief in support of the appeal of the rejection of pending claims 1-10.

I. REAL PARTY IN INTEREST

The real party in interest is PHILIPS SEMICONDUCTOS DRESDEN AG AM WALDSCHLOSSCHEN 1, D-01099 DRESDEN, FEDERAL REPUBLIC OF GERMANY ("PHILIPS"). PHILIPS is the assignee of the entire right, title, and interest in the present application by way of Assignment dated May 19, 2005 recorded on June 1, 2005 at Reel 016615, Frame 0875.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-10 that stand finally rejected. Claims 1, and 4-10 stand rejected under 35 U.S.C. § 103(a) as being obvious from applicant's admission of prior art ("AAPA") and Branstad U.S. patent No. 6,519,716 ("Branstad"). Claims 2 and 3 stand similarly rejected as being obvious from AAPA and Branstad in view of Klein U.S. patent publication No. 2001/0052067.

Claims 1-10 also have been objected to because of informalities noted in claim 1.

The § 103(a) rejections of claims 1-10 are on Appeal.

IV. STATUS OF AMENDMENTS

No after-final amendments have been submitted.

In the pre-Appeal Brief Request for Review, applicants proposed to address the informalities in claim 1 in their next response. Applicants request Examiner's Amendment to claim 1 lines 7-10, at the next appropriate time, as follows: "(a) transferring initialization information for the ~~processor~~ programmable system from an external or internal non-volatile storage medium to an internal memory coupled to the at least one ~~a~~ processor element under the control of a program stored in an instruction memory portion coupled to the at least one processor element."

V. SUMMARY OF CLAIMED SUBJECT MATTER

Applicants' inventive method is directed to the initialization or startup of an ASIC-processor based programmable system in which information required for initializing registers and internal and/or external modules is stored in and read from external memory.

The method, according to claim 1, includes, after turn-on or other event triggering a fresh start of the programmable system, the steps of: (a) transferring initialization information for the [programmable] system from an external or internal non-volatile storage medium to an internal memory coupled to [the at least one] processor element, under the control of a program stored in an instruction memory portion coupled to the [at least one] processor element , wherein the initialization information includes at least one initialization program and initialization data; and (b) reading and transferring initialization data and further initializing the registers and modules under the control of the at least one initialization program transferred into the internal memory portion coupled to the processor element of the programmable system.

The recitations of claim 1 find written support in the specification as follows:

1. A method for initializing a programmable system having at least one processor element, registers and internal and/or external modules, [*Specification ¶ [0016] paragraph lines 1-4*] the method comprising: the steps of:

after turn-on or other event triggering a fresh start of the programmable system [*Specification ¶ [0016] paragraph lines 4-6*],

(a) transferring initialization information for the ~~processor~~ programmable system from an external or internal non-volatile storage medium to an internal memory coupled to a the at least one processor element [*Specification ¶ [0016] paragraph lines 6-8*], under the control of a program stored in an instruction memory portion coupled to the at least one processor element

wherein the initialization information includes at least one initialization program and initialization data [*Specification ¶ [0016] paragraph lines 8-10; ¶[0017] paragraph lines 6-13; etc.*]; and

(b) reading and transferring initialization data and further initializing the registers and modules under the control of the at least one initialization program transferred into the internal memory portion coupled to the processor element of the programmable system [*Specification ¶ [0016] paragraph lines 8-10; ¶[0024] paragraph lines 1-4, etc.*].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection of claims 1 and 4-10 under 35 U.S.C. § 103(a) as being obvious from applicant's admission of prior art ("AAPA") and Branstad U.S. patent No. 6,519,716 ("Branstad").

The similar rejection of claims 2 and 3 as being obvious from AAPA and Branstad in view of Klein U.S. patent publication No. 2001/0052067.

VII. ARGUMENT

The Examiner's has improperly rejected claims 1-10 under 35 U.S.C. § 103(a): claims 1, and 4-10 as being obvious from applicant's admission of prior art ("AAPA") and Branstad U.S. patent No. 6,519,716 ("Branstad"); and, claims 2 and 3 as being obvious from AAPA and Branstad in view of Klein U.S. patent publication No. 2001/0052067. .

The Examiner has improperly rejected claims 1-10 under 35 U.S.C. § 103(a) by failing to make out a proper prima facie case of obviousness.

To establish a prima facie case of obviousness under §103(a), according to MPEP § 2143, three basic criteria must be met: (a) some suggestion or motivation to modify the cited references; (b) a reasonable expectation of success; and (c) a teaching or suggestion of all the elements of claims 1-10.

According to MPEP § 2124 "[t]he initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references. ' Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)."

The §103(a) rejection of claims 1-10 in the Office Action fails to establish a prima facie case of obviousness, at least by failing to provide a convincing line of reasoning as to why

the artisan would have found the claimed invention to have been obvious in light of the teachings of the references

Careful reading of the cited references indicates that their combination does not have any disclosure (explicit or inherent), which shows, teaches, suggests, or provide motivation leading to applicants' inventive method for initialization or startup of an ASIC-processor based programmable system. The Examiner's Rejection is incorrect and should be reversed.

With respect to the prior art rejections, applicants respectfully submit that the Office Action misreads and misapplies both AAPA (the background section of applicants' specification) and Branstad to applicants' claims. The Office Action's reading of Branstad is incorrect and unreasonable in view of a person of ordinary skill in art. Further, the Office Action uses impermissible hindsight in its application of AAPA and Branstad.

Claim 1

Applicants' inventive method, according to claim 1, is directed to the initialization or startup of an ASIC-processor based programmable system in which information required for initializing registers and internal and/or external modules is stored in and read from external memory. The method includes, after turn-on or other event triggering a fresh start of the programmable system, the steps of: (a) transferring initialization information for the processor [programmable] system from an external or internal non-volatile storage medium to an internal memory coupled to [the at least one] processor element, under the control of a program stored in an instruction memory portion coupled to the [at least one] processor element , wherein the initialization information includes at least one initialization program and initialization data; and (b) reading and transferring initialization data and further initializing the registers and modules

under the control of the at least one initialization program transferred into the internal memory portion coupled to the processor element of the programmable system.

Applicants respectfully submit that the steps and arrangement of steps as recited in the claim 1 are not shown, taught, or suggested by AAPA and Branstad even when they are viewed in combination by of a person of ordinary skill in art.

AAPA

AAPA describes a prior art microcontroller-assisted electronic system sold to an OEM customer. (See e.g., specification ¶ [0004]). It is necessary for the OEM customer to a) identify the device, and b) initialize the device by setting the registers with customer specific values or with built in default values. (See e.g., Specification ¶ [0007], [0014], etc.). As described in AAPA, both values for the device identification and the device initialization values may be stored within an EEPROM. The values of the EEPROM are delivered to the respective registers by a specific built in hardware. The specific hardware requires OEM-specific data and data formats. The identification and the initialization as described in the AAPA is not flexible for a usage of the programmable system by other OEM customers. (See e.g., Specification ¶¶ [0009]-[0013], etc.).

Applicants note that the AAPA does not disclose, show, or suggest at least the following elements of claim 1: (a) an internal memory (e.g., instruction RAM 10) coupled to the processor element storing initialization information for the programmable system; (b) the initialization information, which is stored at first in an external or internal non volatile storage medium (14), consisting of initialization data and initialization program; (c) a program stored in an instruction memory (9), which controls the transfer of the initialization information into the instruction

memory; and (d) the initialization program (which was transferred at first into the internal memory) that controls the initialization of the modules and register.

Branstad

Branstad addresses the manner of controlling an operational access time for a non-volatile memory by "Dynamic Memory Testing" to minimize initialization time of an electronic device coupled to a data processing system. (See e.g., Branstad col. 2 lines 32-52, etc.). However, applicants note that Branstad does not describe or teach any method or process for initialization. In fact, Branstad at col. 5, lines 34-35 states that the "the precise program code utilized to implement this functionality [initialization program] is irrelevant." Branstad merely tests suitable initialization conditions i.e., suitable access time for communicating with external memories.

In contrast, claim 1 specifically requires the steps that an initialization program be transferred and stored in the instruction memory portion (e.g., ROM) of the processor element as part of the initialization/startup response. This transferred initialization program then controls the functionality of the processor during system startup including control of the reading of initialization information.

The Office Action, Response to Arguments, §16 cites Branstad col. 1 lines 7-12, which reads:

"FIELD OF THE INVENTION The invention is generally related to the initialization of an electronic device such as an adaptor or other electronically controlled component in a data processing system, and in particular, to control over the retrieval of initialization code for execution by such an electronic device during initialization." The Office Action mistakenly

concludes that this portion of Branstad "teaches the step of transferring an initialization program, ... as claimed." In contrast, claim 1 calls for "a program-controlled" transfer.

Earlier, Office Action § 10 page 4 cites Branstad col. 5 lines 19-24 as teaching " ... transferring initialization program, ... to perform the initialization, ..." This also is inapplicable to claim 1 limitation of "a program-controlled" transfer.

Careful reading shows Branstad at most teaches that a generic prior art initialization code or program, which every processor needs for initialization ("of an electronic device such as an adaptor or other electronically controlled component in a data processing system"), is stored in external nonvolatile storage (EEPROM 58) and retrieved by a (non-programmable) logic block 50. Branstad does not provide any description or details of his initialization program code, which therefore can be no more than prior art initialization program code as understood by a person of skill in the art. Such a person would understand Branstad's prior art initialization process as follows: Microcontroller 42 has an address wherefrom microcontroller 42 after turning on or other event triggering a fresh start, which directs microcontroller 42 to EEPROM 58. The set of instructions for initialization of the adaptor (or other electronically controlled component of the data system) are read from EEPROM 58 via control bus 60 controlled by logic 50. (Branstad differs from AAPA in that the former stores the "initialization program" and latter describes storing "identification data and initialization data" in the EEPROM. This difference is not described in Branstad). Branstad's bus 60 and EEPROM 58 are configured in an unchangeable fixed format, and are therefore comparable with the fixed wired hardware as described in AAPA.

Branstad does not disclose to a person of ordinary skill in the art that "retrieval of initialization code for execution by such an electronic device "is "program controlled" as required by claim 1. This essential feature of claim 1, enables variability of the bus system and the EEPROM. (See e.g., specification ¶[0037]). This inventive "program-controlled" transfer of claim 1 advantageously allows the programmable system to be customized or adapted specifically for OEM customers with different bus/EEPROM types thereby reducing costs.

For at least the foregoing reasons, claim 1 is not obvious from, and is patentable over, the combination of AAPA and Branstad.

Dependent claims 2-10

Dependent claims 2-10 are patentable over the cited references for at least the same reasons parent claim 1 is patentable as discussed above.

VIII. CLAIMS APPENDIX

The rejection of the following claims 1-10 is appealed.

1. A method for initializing a programmable system having at least one processor element, registers and internal and/or external modules, the method comprising: the steps of:

after turn-on or other event triggering a fresh start of the programmable system,

(a) transferring initialization information for the processor system from an external or internal non-volatile storage medium to an internal memory coupled to a processor element, under the control of a program stored in an instruction memory portion coupled to the processor element , wherein the initialization information includes at least one initialization program and initialization data; and

(b) reading and transferring initialization data and further initializing the registers and modules under the control of the at least one initialization program transferred into the internal memory portion coupled to the processor element of the programmable system.

2. The method of claim 1, further characterized in that an integrity check on the initialization information is performed after the transfer, and in that a program branch is carried out under the control of the result of the integrity check.

3. The method of claim 1, further characterized in that, upon identification of an incorrect or missing internal or external storage medium, an error routine is executed which carries out the initialization with standard values or fully or partially restores the content of the internal or external storage medium.

4. The method of claim 1, further characterized in that the initialization data are read as standard values from the storage medium and altered by the processor element, and the altered initialization data are used for initialization.

5. The method of claim 1, further characterized in that the initialization program for the processor element calculates initialization data and uses the calculated data for initialization.

6. The method of claim 5, further characterized in that state data for peripheral components and/or internal components are taken as a basis for calculating the initialization data for these components.

7. The method of claim 1, further characterized in that the processor element changes to a power-saving mode following initialization.

8. The method of claim 1, further characterized in that the initialization of further processor elements is started and monitored.

9. The method of claim 1, further characterized in that adaptation to various storage media is performed.

10. The method of claim 1, further characterized in that the initialization program reloads further data and/or program code from a storage medium.

IX. EVIDENCE APPENDIX

None.

X, RELATED PROCEEDINGS APPENDIX

None.

A33437 065855.0122

For the foregoing reasons, the Examiner' rejection of claims 1- 10 should be reversed

Respectfully submitted,

Dated: November 16, 2007

By: _____

Manu J Tejwani
Patent Office Reg. No. 37,952

Attorney for Appellants
Telephone: (212) 408-2614

Baker Botts L.L.P.
30 ROCKEFELLER Plaza
New York, NY 10112